SESSION 7 – TAPA II
Advanced Interconnects

Wednesday, June 16, 3:25 p.m.
Chairpersons: J. Hutchby, SRC
Y. Takao, Fujitsu

7.1 — 3.25 p.m.
Highly Reliable, 65 nm-node Cu Dual Damascene Interconnects with Full Porous-SiOCH (k=2.5) Films for Low-Power ASICs, M. Ueki, M. Narihiro, H. Ohtake, M. Tagami, M. Tada, F. Ito, Y. Harada, M. Abe, N. Inoue, K. Arai, T. Takeuchi, S. Saito, T. Onodera, N. Furutake, M. Hiroi*, M. Sekine* and Y. Hayashi, NEC Corporation, Kanagawa, Japan and *NEC Electronics Corp., Kanagawa, Japan

Fully-scaled-down, 65nm-node Cu dual damascene interconnects (DDIs) have been developed in full porous-SiOCH films (k=2.5). Two new techniques are introduced such as (1) a low thermal-budget process for securing the DDI via-yield, and (2) a DD pore seal for improving the dielectric reliability. The full porous-SiOCH DDI with the thin Ta/TaN barrier improves the RC productby 24% against the porous-on-rigid, hybrid single damascene interconnects. The cost-effective, DDIs is applicable for the 65nm-node, low-power ASICs.

7.2 — 3:50 p.m.
Integration of Interconnect Process Highly Manufacturable for 65nm CMOS Platform Technology (CMOS5), K. Honda, M. Kanda, R. Ishizuka, Y. Moriuchi, Y. Matsubara, M. Habu, T. Yoshida, S. Matsuda, H. Kittaka, H. Miyajima, T. Hachiya, A. Kajita, T. Usui, N. Nagashima*, R. Kanamura*, Y. Okamoto*, S. Yamada and T. Noguchi, Toshiba Corporation, Yokohama, Japan, *Sony Corporation, Yokohama, Japan

PAE/SiOC/SiC hybrid dual damascene Cu and low-k(k=2.5) interconnect technology for 65nm-node was successfully integrated. The curing condition of the low-kdielectric was selected to maintain enough adhesion strength. Package feasibility test were resulted in successfully. To evaluate influence to the device performance, character of the gate oxide was carefully studied, and resulted in no degradation. In order to demonstrate feasibility for manufacturing, six copper metal layers were fabricated on transistors and memories.

7.3 — 4:15 p.m.
Process Integration of CVD Cu Seed Using ALD Ru Glue Layer for Sub-65nm Cu Interconnect, S.-M. Choi, K.-C. Park, B.-S. Suh, I.-R. Kim, H.-K. Kang, K.-P. Suh, H.-S. Park*, J.-S. Ha* and D.-K. Joo*, Samsung Electronics Co., Ltd., Gyeonggi-Do, Korea, *Genitech, Inc., Daejeon, Korea

CVD Cu was successfully demonstrated as a seed layer for Cu electroplating by using ALD Ru glue layer. The adhesion between barrier metal and CVD Cu was significantly improved by the insertion of Ru. In addition, Ru was found to promote the 2-D planar growth of CVD Cu film rather. Low via resistance was obtained in 0.13μm via chains built in SiOC(k-2.9). CVD Cu seed with ALD Ru is a promising candidate for sub-65nm Cu interconnect.

7.4 — 4:40 p.m.
Reliability Robustness of 65nm BEOL Cu Damascene Interconnects Using Porous CVD Low-k Dielectrics with k = 2.2, K.C. Lin, Y.C. Lu, L.P. Li, B.T. Chen, H.L. Chang, H.H. Lu, S.M. Jeng, S.M. Jang and M.S. Liang, Taiwan Semiconductor Manufacturing Company, Hsin-Chu, Taiwan, ROC

Reliability concerns over the applications of porous low-k dielectrics for Cu dual damascene interconnects have been dismissed with novel film formation methods, patterning approaches and structure designs. Results showed that the BEOL time dependent dielectric breakdown performance of interconnects built using porous CVD LK's with k=2.2 and pore size ~2.8nm are predicted to be $1X10^9$ yrs at 0.3 MV/cm and 125˚C. Further reliability evaluations of the CU/LK in electromigration (EM) and stress migration (SM) showed that its predicted $T_{0.1}$ EM lifetimes for 0.12um Cu lines or 0.13um vias at 1 MA/cm2 and 110˚C are longer than 400K hrs or 150K hrs, and its SM failure rate (>100% shift in Rc) is zero for vias on all test structures after thermal annealing at 150˚C for 500 hrs.

7.5 — 5:05 p.m.
Damage-Free CMP Towards 32nm-node Porous Low-k (k=1.6)/Cu Integration, S. Kondo, B.U. Yoon, S.G. Lee, S. Tokitoh, K. Misawa, T. Yoshie, N. Ohashi and N. Kobayashi, Semiconductor Leading Edge Technologies, Inc., Ibaraki, Japan

To reduce the effective k-value less than 2.6 for the 45nm node, direct CMP of a high-modulus porous MSQ film (k=2.3, E=10GPa) without a protective cap-layer has been applied to 300mm-wafer Cu damascene fabrication by using damage-free CMP. This process can be extended to the 32nm-node ultra low-k (ULK, k=1.6) CMP with a relatively low-k cap-layer by using a newly developed plasma-treatment for promoting adhesion, that supports the low mechanical properties of ULK films (E<1GPa).